APPROVED: /TL/ (03/09/2009)

AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph [0026] of the specification as filed with the following:

[0026] FIGURE 2B illustrates operation of comparator 100 in the fast comparator configuration, but with a pulsed bias current. With the pulsed bias current at a pulse width of 390 nanoseconds (ns), the propagation delay shortens to 0.6 μs for an overdrive voltage V(ov)=±10 mV.

Please replace paragraph [0029] of the specification as filed with the following:

[0029] A pulse generator (not shown in FIGURE 1) coupled to the comparator 100 produces the 390 ~~μs~~ ns bias current pulse. Transistors within comparator 100 are sized for 600 nA of current, and the 2 mV built-in hysteresis and voltage limiting functions are added over existing comparator designs. The analog inputs are expected to reach their steady state before the falling edge of the system clock (clk) signal, where the system clock period is 20 μs and the clock duty cycle is 50%. The pulse generator produces a 390 ns wide pulse on every falling edge of the clk signal, and the comparator output out is sampled with the clk signal's rising edge.